

AMENDMENTS TO THE CLAIMS

Claims 1-20 (Previously Cancelled).

1 / 21. (CURRENTLY AMENDED) A method of fabricating a semiconductor device having a semiconductor region, the method comprising the steps of:

forming at least two conductive posts overlying the semiconductor region by at least a lift-off step to form a structure;

encapsulating the structure and at least one of the at least two conductive posts to form a planarized cured passivation layer; and

exposing the at least one of the at least two conductive posts protrudingly through the planarized cured passivation layer to form the semiconductor device[, wherein the step of forming at least two conductive posts comprises a lift-off step].

2 / 22. (PREVIOUSLY AMENDED) The method of Claim 21, wherein at least one of the at least two conductive posts comprise at least one of Pt, Au and Ti.

3 / 23. (PREVIOUSLY AMENDED) The method of Claim 21, wherein the step of encapsulating the structure and at least one of the at least two conductive posts comprises the steps of:

forming the passivation layer by spinning on benzocyclobutene ("BCB"); and

heating the passivation layer in an N₂ atmosphere to a temperature substantially in the range of 250-350°C for a period substantially in the range of 1-30 minutes, the passivation layer spun on, cured and planarized.

4/ 24. (ORIGINAL) The method of Claim 21, wherein the step of exposing the at least one of the at least two conductive posts comprises the step of etching the planarized cured passivation layer.

25. (PREVIOUSLY AMENDED) The method of Claim 32, wherein the Reactive Ion Etching step employs a chemistry of at least one of CF₄:O₂ at an approximate ratio of 40:60 and SF₆:O₂ at an approximate ratio of 6:10.

5 26. (CURRENTLY AMENDED) A method of fabricating a semiconductor device having a semiconductor region, the method comprising the steps of:

forming at least two conductive posts of about the same height by at least a lift-off step overlying the semiconductor region to form a structure;

encapsulating the structure and [at least one of] the at least two conductive posts to form a planarized cured passivation layer; and

exposing the [at least one of] the at least two conductive posts protrudingly through the planarized cured passivation layer to form the semiconductor device[, wherein the step of forming at least two conductive posts comprises a lift-off step].

6 27. (PREVIOUSLY AMENDED) The method of Claim 26, wherein at least one of the at least two conductive posts comprises at least one of Pt, Au and Ti.

7 28. (PREVIOUSLY AMENDED) The method of Claim 26, wherein the step of encapsulating the structure and at least one of the at least two conductive posts comprises the steps of:

forming the passivation layer by spinning on benzocyclobutene ("BCB"); and

heating the passivation layer in an N₂ atmosphere to a temperature substantially in the range of 250-350°C for a period substantially in the range of 1-30 minutes, the passivation layer spun on, cured and planarized.

8 29. (ORIGINAL) The method of Claim 26, wherein the step of exposing the at least one of the at least two conductive posts comprises the step of etching the planarized cured passivation layer.

9 30. (PREVIOUSLY AMENDED) The method of Claim 29, wherein the step of etching the planarized cured passivation layer comprises a Reactive Ion Etching step.

10 31. (PREVIOUSLY AMENDED) The method of Claim 30, wherein the Reactive Ion Etching step employs a chemistry of at least one of CF₄:O₂ at an approximate ratio of 40:60 and SF₆:O₂ at an approximate ratio of 6:10.

1.1 32. (PREVIOUSLY ENTERED) The method of Claim 24, wherein the step of etching the planarized cured passivation layer comprises a Reactive Ion Etching step.

1.2 33. (NEW) The method of Claim 21, wherein the step of exposing reduces a height of the planarized cured passivation layer beneath or equal to a height of the at least one of the at least two conductive posts.

1.3 34. (NEW) The method of Claim 26, wherein the step of exposing reduces a height of the planarized cured passivation layer beneath or equal to a height of the at least one of the at least two conductive posts.

1.5 35. (NEW) A method of fabricating a semiconductor device having a semiconductor region, the method comprising the steps of:

forming at least one conductive post overlying the semiconductor region to form a structure;

encapsulating the structure and the at least one conductive post to form a planarized cured passivation layer; and

etching the planarized cured passivation layer causing the encapsulated at least one conductive post to protrude through the planarized cured passivation layer and form the semiconductor device.

16 36. (NEW) The method of Claim 35, wherein the step of etching reduces a height of the planarized cured passivation layer beneath or equal to a height of the at least one conductive post.

17 37. (NEW) The method of Claim 36, wherein the step of etching comprises:

masking a portion of the encapsulated structure, the portion corresponding with a position of the encapsulated at least one conductive post.